

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use **<http://www.nexperia.com>**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

74ABT544

Octal latched transceiver with dual enable; 3-state

Rev. 6 — 3 November 2011

Product data sheet

1. General description

The 74ABT544 high performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 octal latched transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$) and output enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64 mA.

2. Features and benefits

- Combines 74ABT640 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Live insertion and extraction permitted
- Output capability: +64 mA to –32 mA
- Power-up 3-state
- Power-up reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

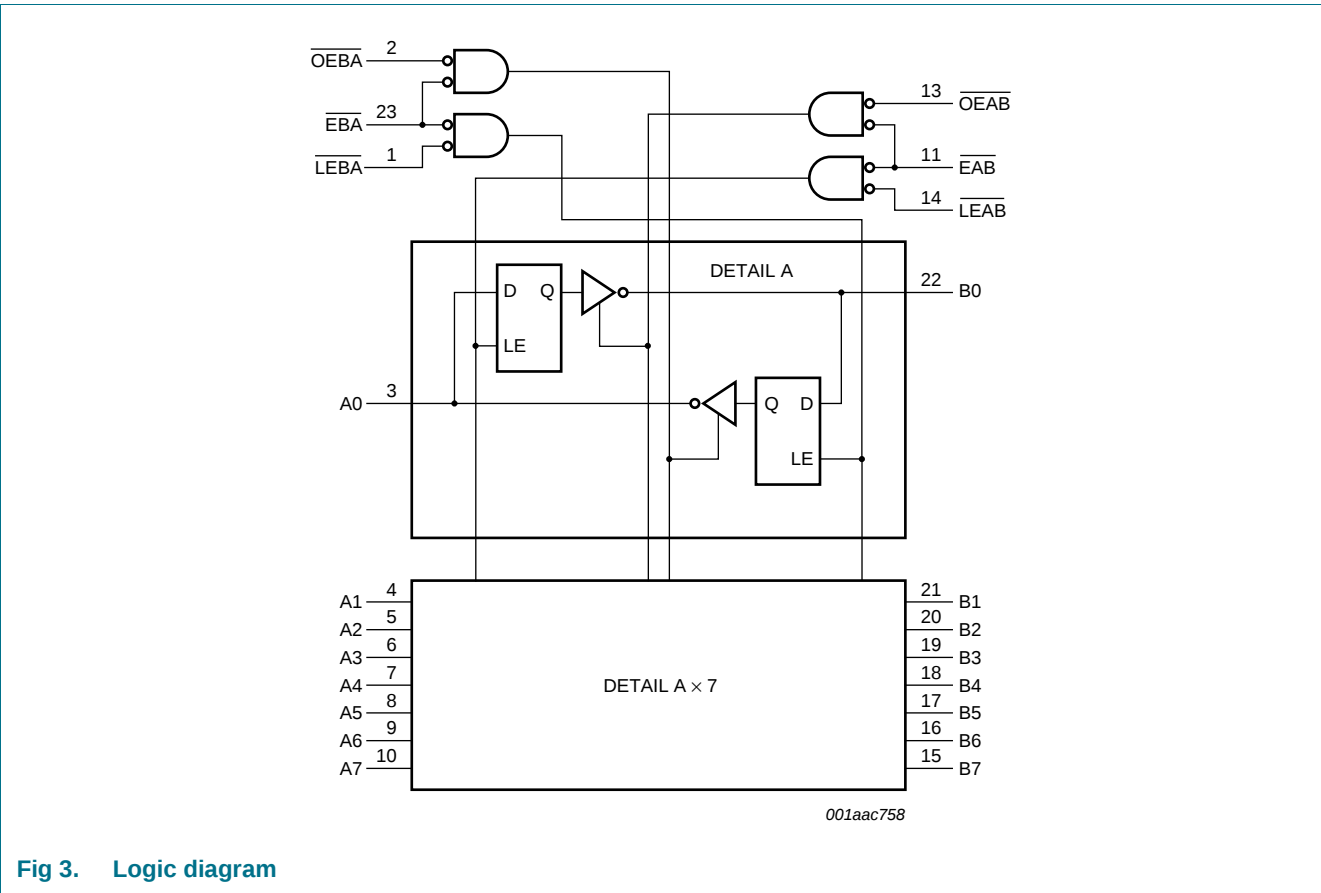
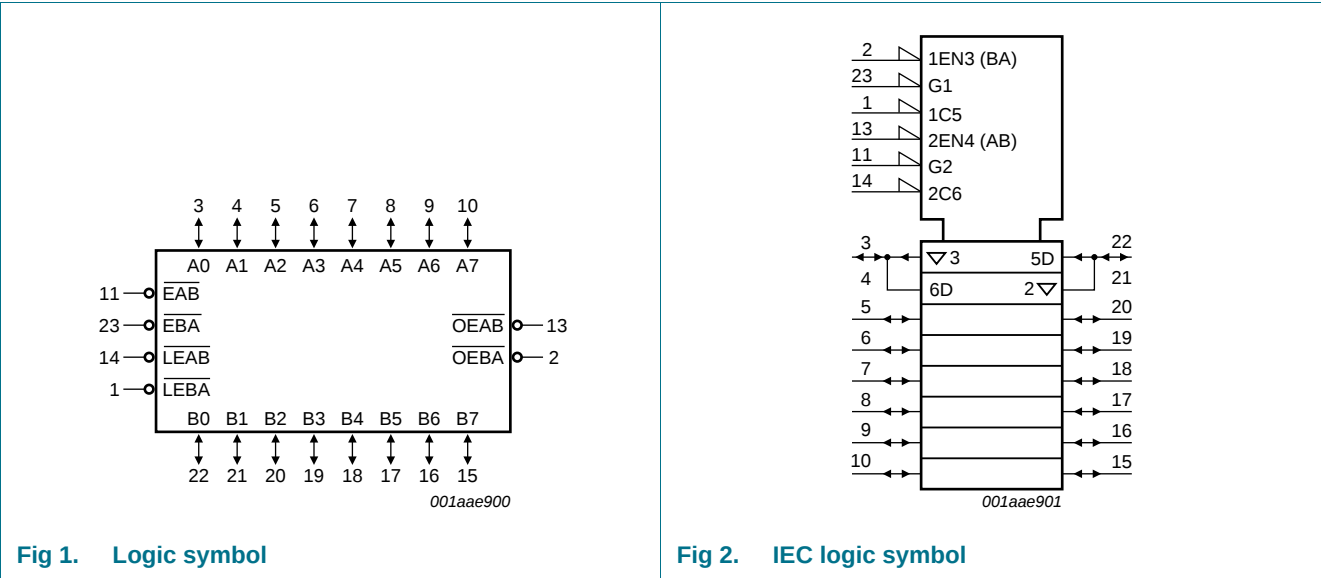
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT544D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT544DB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT544PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

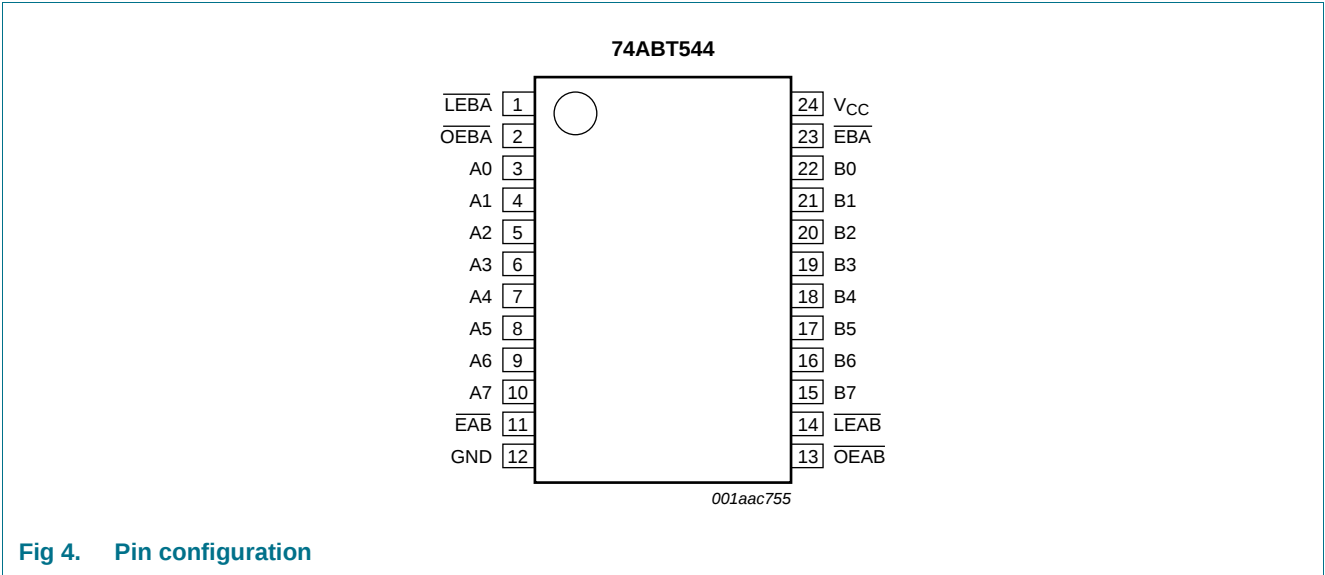


4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
LEBA	1	B-to-A latch enable input (active LOW)
OEBA	2	B-to-A output enable input (active LOW)
A0 to A7	3, 4, 5, 6, 7, 8, 9, 10	data input or output
EAB	11	A-to-B enable input (active LOW)
GND	12	ground (0 V)
OEAB	13	A-to-B output enable input (active LOW)
LEAB	14	A-to-B latch enable input (active LOW)
B0 to B7	22, 21, 20, 19, 18, 17, 16, 15	data input or output
EBA	23	B-to-A enable input (active LOW)
V _{CC}	24	positive supply voltage

6. Functional description

6.1 Function table

Table 3. Function selection^[1]

Input				Output	Status
OEXX	EXX	LEXX	An or Bn	Bn or An	
H	X	X	X	Z	disabled
X	H	X	X	Z	
L	↑	L	h	Z	disabled + latch
			l	Z	
L	L	↑	h	L	latch + display
			l	H	
L	L	L	H	L	transparent
			L	H	
L	L	H	X	NC	hold

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
 ↑ = LOW-to-HIGH clock transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX = AB or BA);
 NC = no change;
 X = don't care;
 Z = high-impedance OFF-state.

6.2 Description

The 74ABT544 contains two sets of eight D-type latches, with separate control pins for each set.

Using data flow from A-to-B as an example, when the A-to-B enable ($\overline{\text{EAB}}$) input, the A-to-B latch enable ($\overline{\text{LEAB}}$) input and the A-to-B output enable ($\overline{\text{OEAB}}$) input are all LOW, the A-to-B path is transparent.

A subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B-to-A is similar, but using the $\overline{\text{EBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		^[1] -1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	^[1] -0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
T_j	junction temperature		^[2] -	150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5$ V; $I_{IK} = -18$ mA	-1.2	-0.9	-	-1.2	-	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_{IH}						
		$V_{CC} = 4.5$ V; $I_{OH} = -3$ mA	2.5	3.2	-	2.5	-	V
		$V_{CC} = 5.0$ V; $I_{OH} = -3$ mA	3.0	3.7	-	3.0	-	V
		$V_{CC} = 4.5$ V; $I_{OH} = -32$ mA	2.0	2.3	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5$ V; $I_{OL} = 64$ mA; $V_I = V_{IL}$ or V_{IH}	-	0.42	0.55	-	0.55	V

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 5.5 \text{ V}$; $I_O = 1 \text{ mA}$; $V_I = \text{GND or } V_{CC}$ [1]	-	0.13	0.55	-	0.55	V
I_I	input leakage current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } 5.5 \text{ V}$						
		control pins	-	± 0.01	± 1.0	-	± 1.0	μA
		An, Bn	-	± 5.0	± 100	-	± 100	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}$; V_I or $V_O \leq 4.5 \text{ V}$	-	± 5.0	± 100	-	± 100	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.1 \text{ V}$; $V_O = 0.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$; OEAB, OEBA don't care [2]	-	± 5.0	± 50	-	± 50	μA
I_{OZ}	OFF-state output current	$V_{CC} = 5.5 \text{ V}$; $V_I = V_{IL}$ or V_{IH}						
		$V_O = 2.7 \text{ V}$	-	5.0	50	-	50	μA
		$V_O = 0.5 \text{ V}$	-	-5.0	-50	-	-50	μA
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$	-	5.0	50	-	50	μA
I_O	output current	$V_{CC} = 5.5 \text{ V}$; $V_O = 2.5 \text{ V}$ [3]	-180	-65	-50	-180	-50	mA
I_{CC}	supply current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$						
		outputs HIGH-state	-	110	250	-	250	μA
		outputs LOW-state	-	20	30	-	30	mA
		outputs disabled	-	110	250	-	250	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V}$; one input pin at 3.4 V, other inputs at V_{CC} or GND [4]	-	0.3	1.5	-	1.5	mA
C_I	input capacitance	$V_I = 0 \text{ V or } V_{CC}$	-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; $V_O = 0 \text{ V or } V_{CC}$	-	7	-	-	-	pF

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From $V_{CC} = 2.1 \text{ V}$ to $V_{CC} = 5 \text{ V} \pm 10 \%$, a transition time of up to 100 μs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

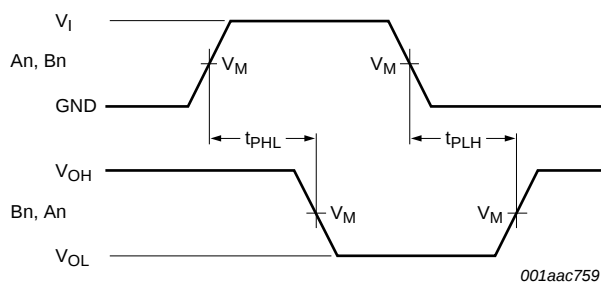
Table 7. Dynamic characteristics
 GND = 0 V; for test circuit, see Figure 10.

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0 \text{ V}$			–40 °C to +85 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An; see Figure 5	1.7	3.0	3.8	1.7	4.7	ns
		LEBA to An or LEAB to Bn; see Figure 6	2.1	3.5	4.2	2.1	5.2	ns

Table 7. Dynamic characteristics ...continuedGND = 0 V; for test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			–40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An; see Figure 5	2.4	3.6	4.5	2.4	5.2	ns
		$\overline{\text{LEBA}}$ to An or $\overline{\text{LEAB}}$ to Bn; see Figure 6	3.0	4.4	5.3	3.0	6.2	ns
t _{PZH}	OFF-state to HIGH propagation delay	$\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 7	1.8	3.0	3.9	1.8	4.7	ns
		$\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 7	1.9	3.4	4.1	1.9	5.0	ns
t _{PZL}	OFF-state to LOW propagation delay	$\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 8	2.9	4.2	5.2	2.9	6.1	ns
		$\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 8	3.1	4.6	5.5	3.1	6.5	ns
t _{PHZ}	HIGH to OFF-state propagation delay	$\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 7	2.0	3.3	4.3	2.0	4.9	ns
		$\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 7	2.1	3.4	4.5	2.1	5.2	ns
t _{PLZ}	LOW to OFF-state propagation delay	$\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn; see Figure 8	2.0	2.8	5.8	2.0	6.3	ns
		$\overline{\text{EBA}}$ to An, $\overline{\text{EAB}}$ to Bn; see Figure 8	2.0	3.0	6.2	2.0	6.7	ns
t _{SU(H)}	set-up time HIGH	An to $\overline{\text{LEAB}}$, Bn to $\overline{\text{LEBA}}$; see Figure 9	3.0	1.5	-	3.0	-	ns
		An to $\overline{\text{EAB}}$, Bn to $\overline{\text{EBA}}$; see Figure 9	3.0	1.5	-	3.0	-	ns
t _{SU(L)}	set-up time LOW	An to $\overline{\text{LEAB}}$, Bn to $\overline{\text{LEBA}}$; see Figure 9	3.0	0.6	-	3.0	-	ns
		An to $\overline{\text{EAB}}$, Bn to $\overline{\text{EBA}}$; see Figure 9	3.0	0.6	-	3.0	-	ns
t _{h(H)}	hold time HIGH	$\overline{\text{LEAB}}$ to An, $\overline{\text{LEBA}}$ to Bn; see Figure 9	+0.5	–0.3	-	0.5	-	ns
		$\overline{\text{EAB}}$ to An, $\overline{\text{EBA}}$ to Bn; see Figure 9	+0.5	–0.2	-	0.5	-	ns
t _{h(L)}	hold time LOW	$\overline{\text{LEAB}}$ to An, $\overline{\text{LEBA}}$ to Bn; see Figure 9	+0.5	–1.3	-	0.5	-	ns
		$\overline{\text{EAB}}$ to An, $\overline{\text{EBA}}$ to Bn; see Figure 9	+0.5	–1.3	-	0.5	-	ns
t _{WL}	pulse width LOW	latch enable; see Figure 9	3.5	1.8	-	3.5	-	ns

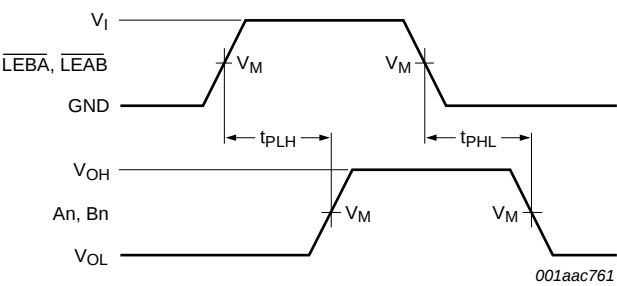
11. Waveforms



$V_M = 1.5 \text{ V}$

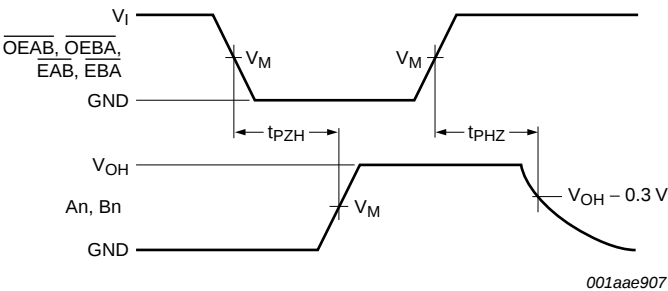
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (An, Bn) to output (Bn, An)



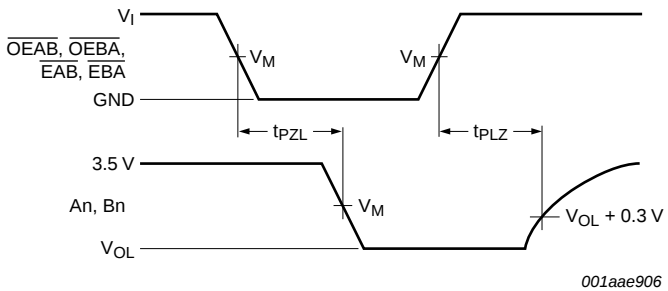
$V_M = 1.5\text{ V}$
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay latch enable ($\overline{LEAB}, \overline{LEBA}$) to output (An, Bn)



$V_M = 1.5\text{ V}$
 V_{OH} is a typical voltage output level that occurs with the output load.

Fig 7. Propagation delay 3-state output enable to HIGH-level and output disable from HIGH-level



$V_M = 1.5\text{ V}$
 V_{OL} is a typical voltage output level that occurs with the output load.

Fig 8. Propagation delay 3-state output enable to LOW-level and output disable from LOW-level

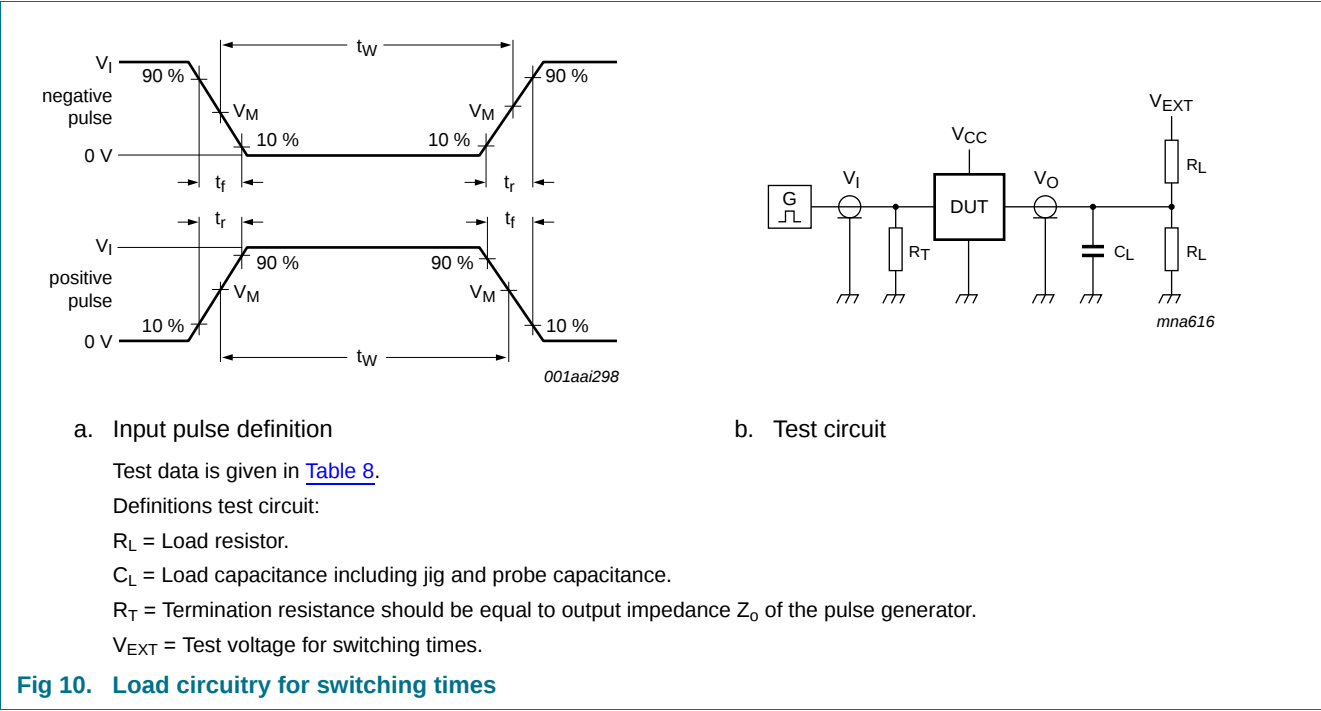
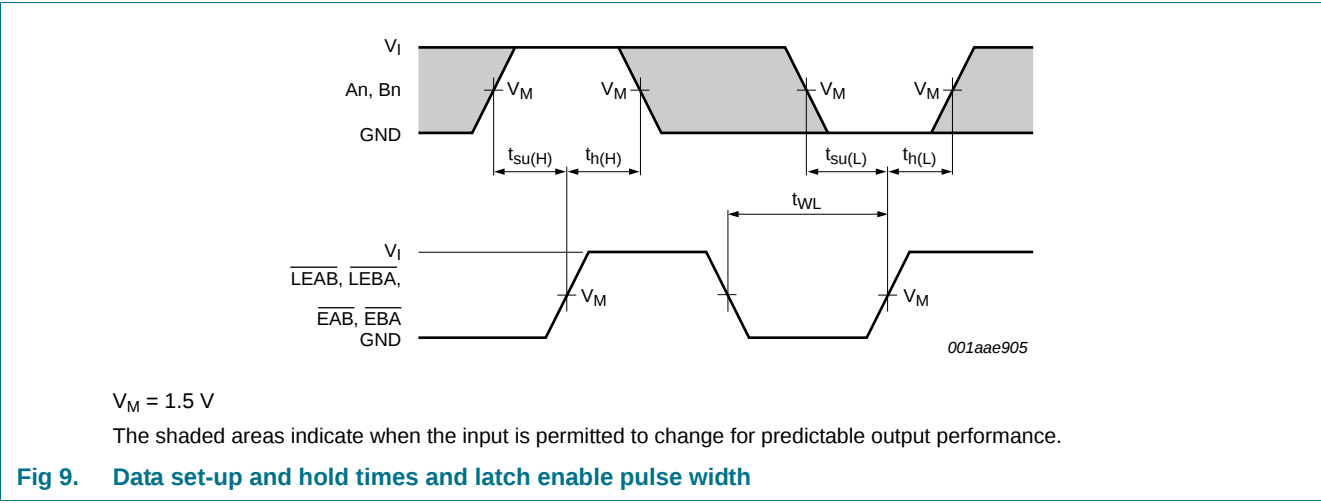


Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

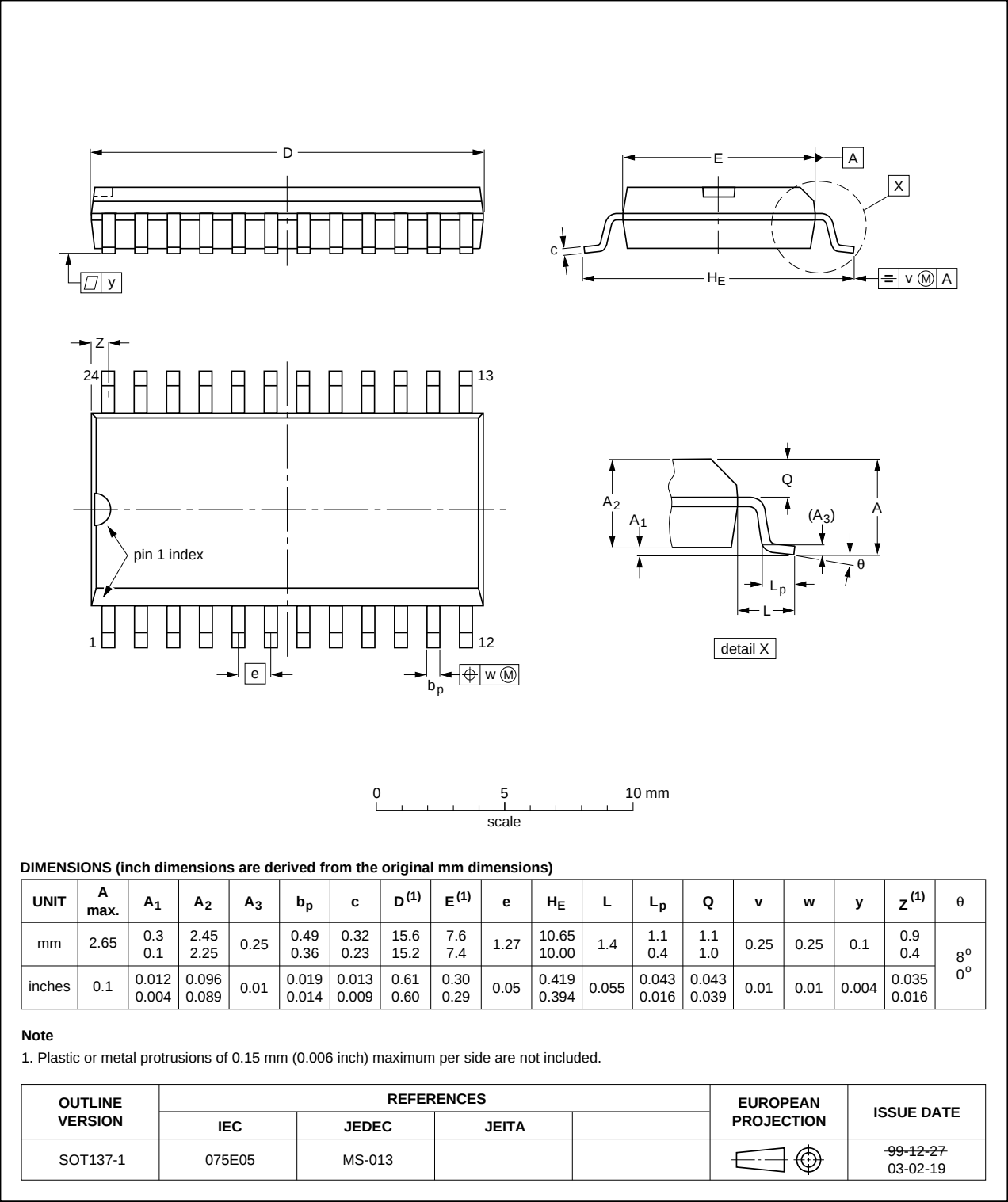


Fig 11. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

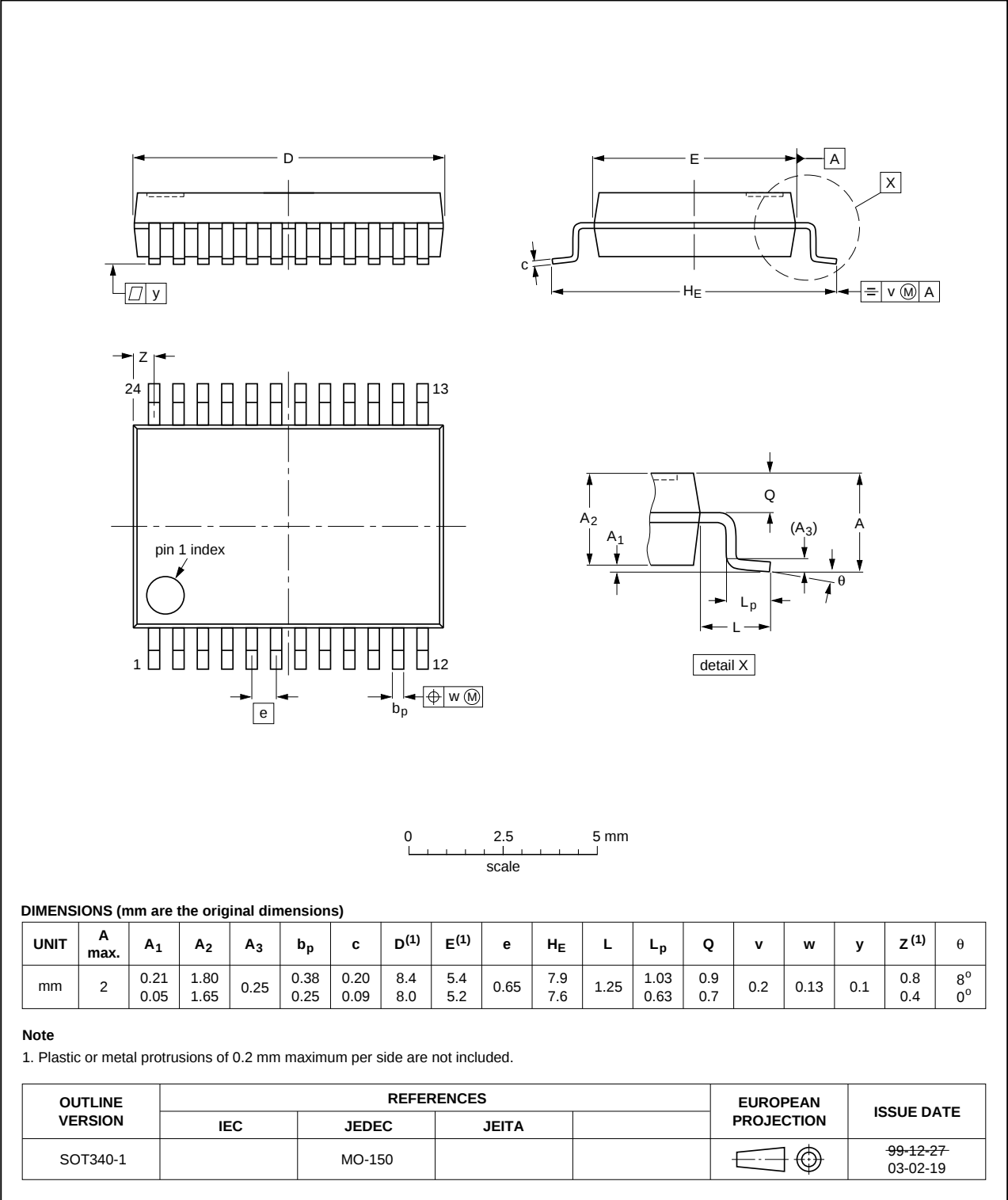


Fig 12. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

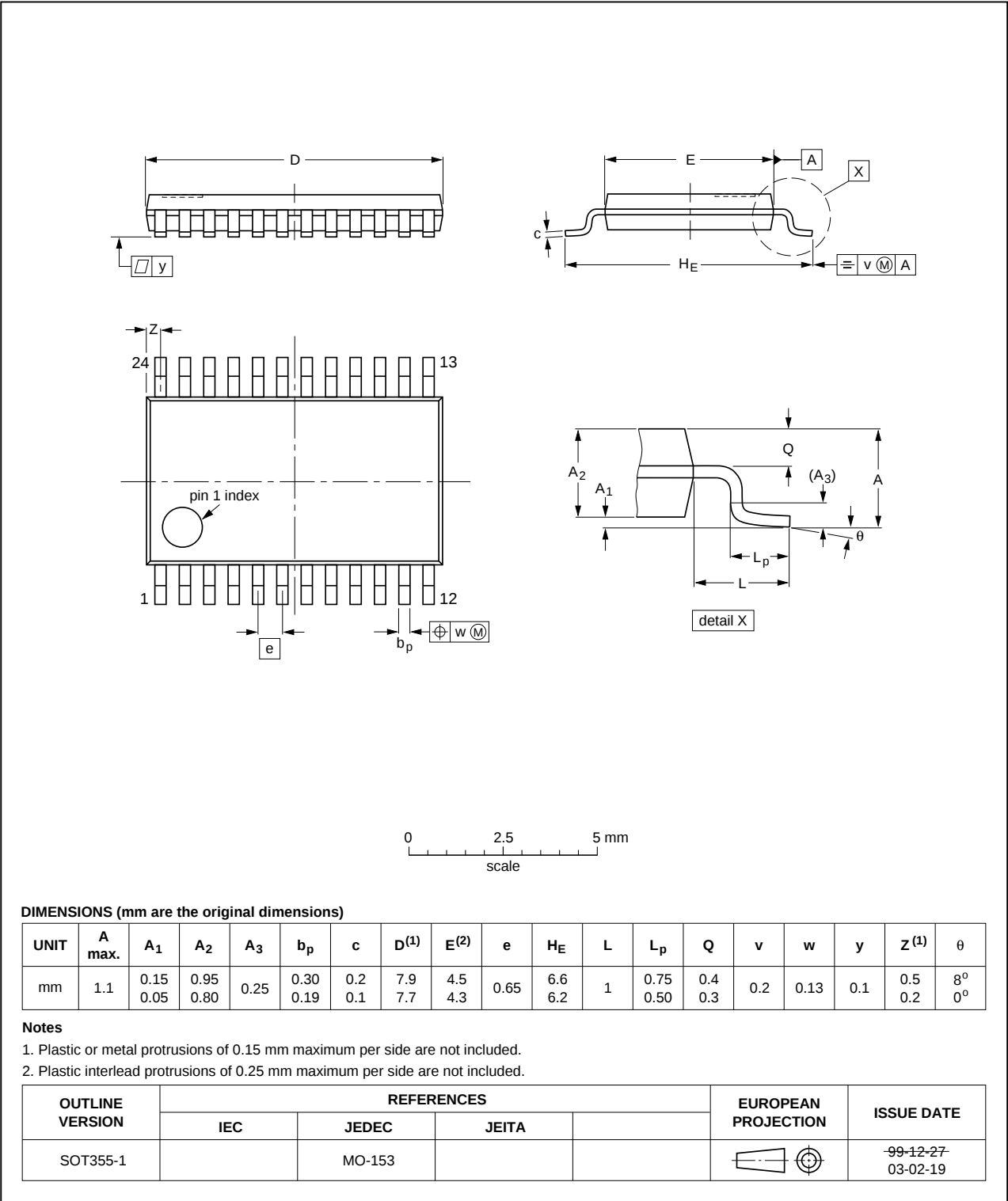


Fig 13. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT544 v.6	20111103	Product data sheet	-	74ABT544 v.5
Modifications:	• Legal pages updated			
74ABT544 v.5	20100520	Product data sheet	-	74ABT544 v.4
74ABT544 v.4	20100115	Product data sheet	-	74ABT544 v.3
74ABT544 v.3	20050420	Product specification	-	74ABT544 v.2
74ABT544 v.2	20021118	Product specification	-	74ABT544
74ABT544	19930701	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
6.1	Function table	4
6.2	Description	4
7	Limiting values	5
8	Recommended operating conditions	5
9	Static characteristics	5
10	Dynamic characteristics	6
11	Waveforms	7
12	Package outline	10
13	Abbreviations	13
14	Revision history	13
15	Legal information	14
15.1	Data sheet status	14
15.2	Definitions	14
15.3	Disclaimers	14
15.4	Trademarks	15
16	Contact information	15
17	Contents	16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 3 November 2011

Document identifier: 74ABT544